CMOS SuperSync FIFO™
8,192 x 18
16,384 x 18

IDT72255LA
IDT72265LA

FEATURES

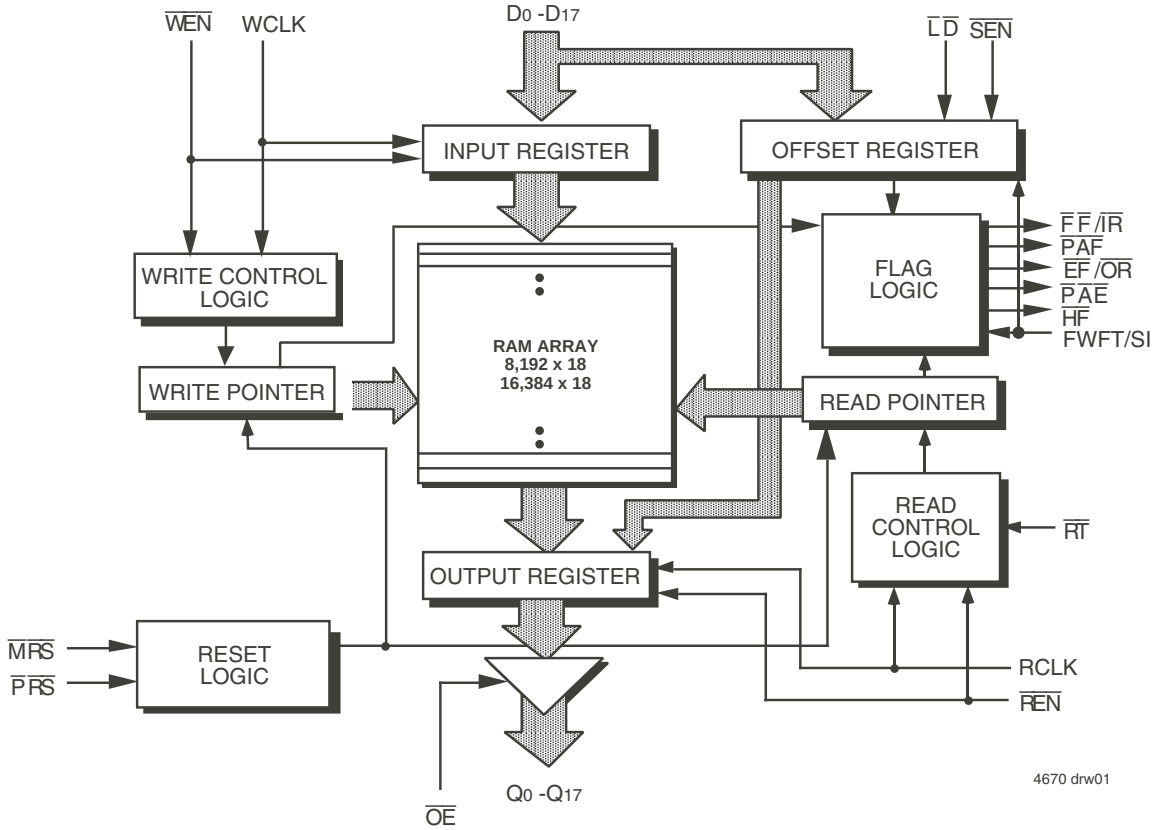
- **Choose among the following memory organizations:**
  IDT72255LA — 8,192 x 18
  IDT72265LA — 16,384 x 18
- **Pin-compatible with the IDT72275/72285 SuperSync FIFOs**
- **10ns read/write cycle time (8ns access time)**
- **Fixed, low first word data latency time**
- **Auto power down minimizes standby power consumption**
- **Master Reset clears entire FIFO**
- **Partial Reset clears data, but retains programmable settings**
- **Retransmit operation with fixed, low first word data latency time**
- **Empty, Full and Half-Full flags signal FIFO status**
- **Programmable Almost-Empty and Almost-Full flags, each flag can default to one of two preselected offsets**
- **Program partial flags by either serial or parallel means**
- **Select IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$ flags) or First Word Fall Through timing (using $\overline{OR}$ and $\overline{IR}$ flags)**
- **Output enable puts data outputs into high impedance state**
- **Easily expandable in depth and width**
- **Independent Read and Write clocks (permit reading and writing simultaneously)**
- **Available in the 64-pin Thin Quad Flat Pack (TQFP) and the 64-pin Slim Thin Quad Flat Pack (STQFP)**
- **High-performance submicron CMOS technology**
- **Industrial temperature range (–40°C to +85°C) is available**
- **Green parts available, see ordering information**

DESCRIPTION

The IDT72255LA/72265LA are exceptionally deep, high speed, CMOS First-In-First-Out (FIFO) memories with clocked read and write controls. These FIFOs offer numerous improvements over previous SuperSync FIFOs, including the following:

- The limitation of the frequency of one clock input with respect to the other has been removed. The Frequency Select pin (FS) has been removed, thus it is no longer necessary to select which of the two clock inputs, RCLK or WCLK, is running at the higher frequency.
- The period required by the retransmit operation is now fixed and short.
- The first word data latency period, from the time the first word is written to an empty FIFO to the time it can be read, is now fixed and short. (The variable clock cycle counting delay associated with the latency period found on previous SuperSync devices has been eliminated on this SuperSync family.)

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION (CONTINUED)

SuperSync FIFOs are particularly appropriate for networking, video, telecommunications, data communications and other applications that need to buffer large amounts of data.

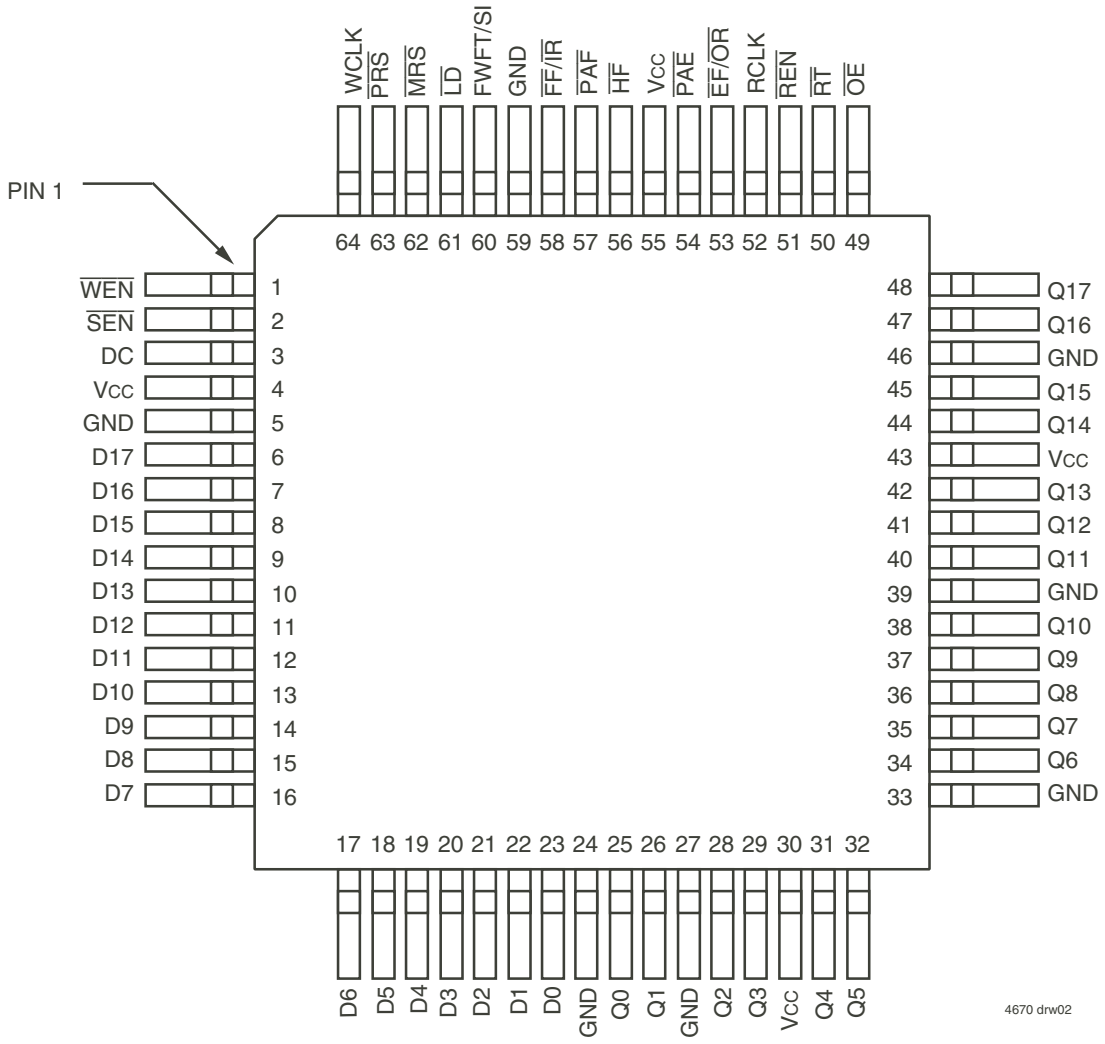
The input port is controlled by a Write Clock (WCLK) input and a Write Enable ($\overline{WEN}$) input. Data is written into the FIFO on every rising edge of WCLK when $\overline{WEN}$ is asserted. The output port is controlled by a Read Clock (RCLK) input and Read Enable ($\overline{REN}$) input. Data is read from the FIFO on every rising edge of RCLK when $\overline{REN}$ is asserted. An Output Enable ($\overline{OE}$) input is provided for three-state control of the outputs.

The frequencies of both the RCLK and the WCLK signals may vary from 0 to f_{MAX} with complete independence. There are no restrictions on the frequency of one clock input with respect to the other.

There are two possible timing modes of operation with these devices: IDT Standard mode and First Word Fall Through (FWFT) mode.

In *IDT Standard mode*, the first word written to an empty FIFO will not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating $\overline{REN}$ and enabling a rising RCLK edge, will shift the word from internal memory to the data output lines.

PIN CONFIGURATIONS



TQFP (PN64-1, ORDER CODE: PF)
STQFP (PP64-1, ORDER CODE: TF)
TOP VIEW

NOTE:
1. DC = Don't Care. Must be tied to GND or V_{CC}, cannot be left open.

DESCRIPTION (CONTINUED)

In *FWFT mode,* the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. A $\overline{REN}$ does not have to be asserted for accessing the first word. However, subsequent words written to the FIFO do require a LOW on $\overline{REN}$ for access. The state of the FWFT/SI input during Master Reset determines the timing mode in use.

For applications requiring more data storage capacity than a single FIFO can provide, the FWFT timing mode permits depth expansion by chaining FIFOs in series (i.e. the data outputs of one FIFO are connected to the corresponding data inputs of the next). No external logic is required.

These FIFOs have five flag pins, $\overline{EF}$/$\overline{OR}$ (Empty Flag or Output Ready), $\overline{FF}$/$\overline{IR}$ (Full Flag or Input Ready), $\overline{HF}$ (Half-full Flag), $\overline{PAE}$ (Programmable Almost-Empty flag) and $\overline{PAF}$ (Programmable Almost-Full flag). The $\overline{EF}$ and $\overline{FF}$ functions are selected in IDT Standard mode. The $\overline{IR}$ and $\overline{OR}$ functions are selected in FWFT mode. $\overline{HF}$, $\overline{PAE}$ and $\overline{PAF}$ are always available for use, irrespective of timing mode.

$\overline{PAE}$ and $\overline{PAF}$ can be programmed independently to switch at any point in memory. (See Table I and Table 2.) Programmable offsets determine the flag switching threshold and can be loaded by two methods: parallel or serial. Two default offset settings are also provided, so that $\overline{PAE}$ can be set to switch at 127 or 1,023 locations from the empty boundary and the $\overline{PAF}$ threshold can be set at 127 or 1,023 locations from the full boundary. These choices are made with the $\overline{LD}$ pin during Master Reset.

For serial programming, $\overline{SEN}$ together with $\overline{LD}$ on each rising edge of WCLK, are used to load the offset registers via the Serial Input (SI). For parallel programming, $\overline{WEN}$ together with $\overline{LD}$ on each rising edge of WCLK, are used to load the offset registers via Dn. $\overline{REN}$ together with $\overline{LD}$ on each rising edge of RCLK can be used to read the offsets in parallel from Qn regardless of whether serial or parallel offset loading has been selected.

During Master Reset ($\overline{MRS}$) the following events occur: The read and write pointers are set to the first location of the FIFO. The FWFT pin selects IDT Standard mode or FWFT mode. The $\overline{LD}$ pin selects either a partial flag default setting of 127 with parallel programming or a partial flag default setting of 1,023 with serial programming. The flags are updated according to the timing mode and default offsets selected.

The Partial Reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the timing mode, partial flag programming method, and default or programmed offset settings existing before Partial Reset remain unchanged. The flags are updated according to the timing mode and offsets in effect. $\overline{PRS}$ is useful for resetting a device in mid-operation, when reprogramming partial flags would be undesirable.

The Retransmit function allows data to be reread from the FIFO more than once. A LOW on the $\overline{RT}$ input during a rising RCLK edge initiates a retransmit operation by setting the read pointer to the first location of the memory array.

If, at any time, the FIFO is not actively performing an operation, the chip will automatically power down. Once in the power down state, the standby supply current consumption is minimized. Initiating any operation (by activating control inputs) will immediately take the device out of the power down state.

The IDT72255LA/72265LA are fabricated using IDT's high speed submicron CMOS technology.

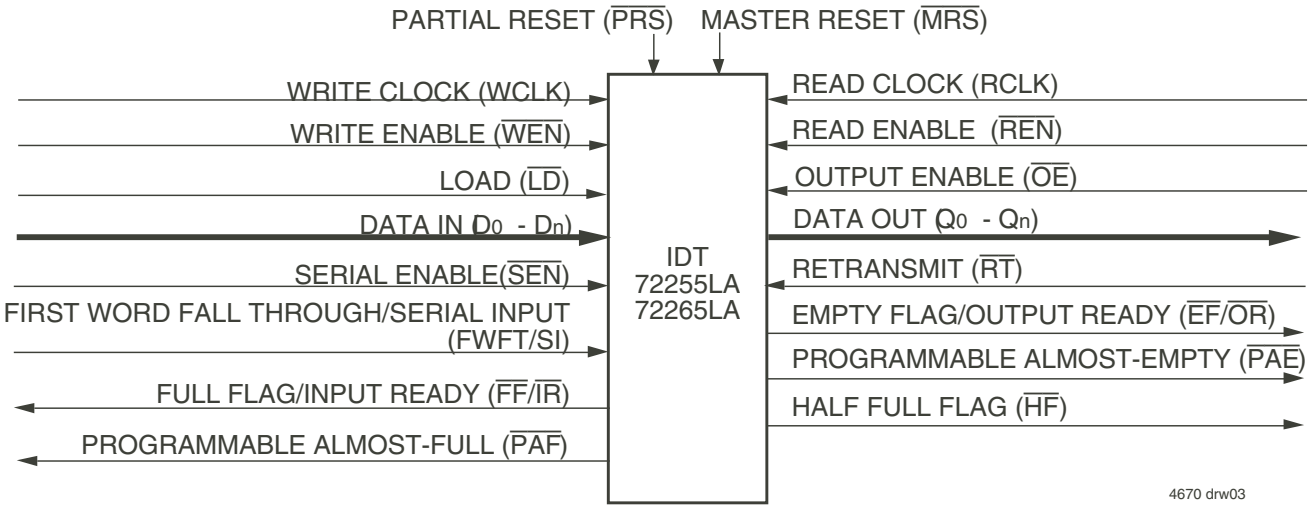


Figure 1. Block Diagram of Single 8,192 x 18 and 16,384 x 18 Synchronous FIFO

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	° C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (Com'l/Ind'l)	4.0	5.0	5.5	V
GND	Supply Voltage (Com'l/Ind'l)	0	0	0	V
V_{IH}	Input High Voltage (Com'l/Ind'l)	2.0	—	—	V
V_{IL}[1]	Input Low Voltage (Com'l/Ind'l)	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	+70	°C
T_A	Operating Temperature Industrial	-40	—	+85	°C

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Industrial: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C)

Symbol	Parameter	IDT72255LA IDT72265LA Commercial & Industrial[1] t_{CLK} = 10, 15, 20 ns		Unit
		Min.	Max.	
I_{LI}[2]	Input Leakage Current	–1	1	µA
I_{LO}[3]	Output Leakage Current	–10	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	0.4	V
I_{CC1}[4,5,6]	Active Power Supply Current	—	80	mA
I_{CC2}[4,7]	Standby Current	—	20	mA

NOTES:
1. Industrial temperature range product for 15ns and 20ns speed grades are available as a standard device.
2. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
3. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
4. Tested with outputs disabled (I_{OUT} = 0).
5. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
6. Typical I_{CC1} = 15 + 2.1*fs + 0.02*C_L*fs (in mA) with V_{CC} = 5V, T_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
7. All Inputs = V_{CC} –0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:
1. With output deselected, ($\overline{OE}$ ≥ V_{IH}).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS(1)

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Industrial: VCC = 5V ± 10%, TA = –40°C to +85°C)

		Commercial		Commercial & Industrial(2)				
		IDT72255LA10 IDT72265LA10		IDT72255LA15 IDT72265LA15		IDT72255LA20 IDT72265LA20		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	100	—	66.7	—	50	MHz
tA	Data Access Time	2	8	2	10	2	12	ns
tCLK	Clock Cycle Time	10	—	15	—	20	—	ns
tCLKH	Clock High Time	4.5	—	6	—	8	—	ns
tCLKL	Clock Low Time	4.5	—	6	—	8	—	ns
tDS	Data Setup Time	3	—	4	—	5	—	ns
tDH	Data Hold Time	0	—	1	—	1	—	ns
tENS	Enable Setup Time	3	—	4	—	5	—	ns
tENH	Enable Hold Time	0	—	1	—	1	—	ns
tLDS	Load Setup Time	3	—	4	—	5	—	ns
tLDH	Load Hold Time	0	—	1	—	1	—	ns
tRS	Reset Pulse Width(3)	10	—	15	—	20	—	ns
tRSS	Reset Setup Time	10	—	15	—	20	—	ns
tRSR	Reset Recovery Time	10	—	15	—	20	—	ns
tRSF	Reset to Flag and Output Time	—	10	—	15	—	20	ns
tFWFT	Mode Select Time	0	—	0	—	0	—	ns
tRTS	Retransmit Setup Time	3	—	4	—	5	—	ns
tOLZ	Output Enable to Output in Low Z(4)	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	2	6	3	8	3	10	ns
tOHZ	Output Enable to Output in High Z(4)	2	6	3	8	3	10	ns
tWFF	Write Clock to $\overline{FF}$ or $\overline{IR}$	—	8	—	10	—	12	ns
tREF	Read Clock to $\overline{EF}$ or $\overline{OR}$	—	8	—	10	—	12	ns
tPAF	Write Clock to $\overline{PAF}$	—	8	—	10	—	12	ns
tPAE	Read Clock to $\overline{PAE}$	—	8	—	10	—	12	ns
tHF	Clock to $\overline{HF}$	—	16	—	20	—	22	ns
tSKEW1	Skew time between RCLK and WCLK for $\overline{FF}$/$\overline{IR}$	5	—	6	—	10	—	ns
tSKEW2	Skew time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	12	—	15	—	20	—	ns
tSKEW3	Skew time between RCLK and WCLK for $\overline{EF}$/$\overline{OR}$	60	—	60	—	60	—	ns
tSKEW4	Skew time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$ for Re-transmit operation	15	—	17	—	25	—	ns

NOTES:
1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Industrial temperature range product for 15ns and 20ns speed grades are available as a standard device.
3. Pulse widths less than minimum values are not allowed.
4. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 2

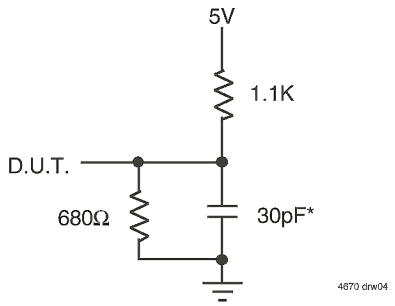
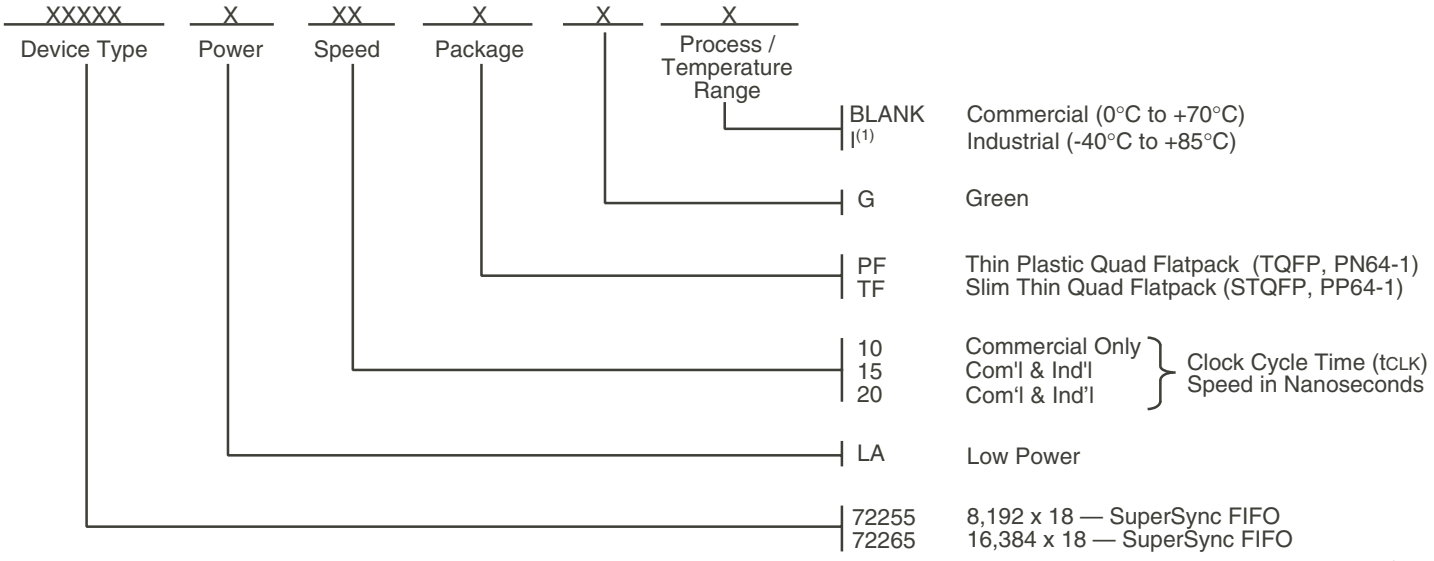


Figure 2. Output Load

* Includes jig and scope capacitances.

ORDERING INFORMATION



4670 drw24

NOTES:

1. Industrial temperature range product for 15ns and 20ns speed grades are available as a standard device.
2. Green parts available. For specific speeds and packages contact your sales office.